Simplify your MIL-STD-1553 Design Implementation… with a fast Serial Peripheral Interface (SPI) Controller

The migration towards a System on Chip (SoC) approach to electronics systems is a growing trend within the military aerospace industry, driven primarily by a desire to reduce size, weight and power (SWaP), and to accommodate the requirements of complex avionics systems, which typically require a myriad of unique I/O interfaces between embedded computing resources, sensors, and effectors. Today's latest generation FPGA's offer a combination of computing cores, with large amounts of programmable logic, therefore it may seem tempting to implement a MIL-STD-1553 SoC solution utilizing an FPGA. But is an FGPA implementation of the 1553 controller the best approach? As an alternative, and simplified option, we will explore the use of a MIL-STD-1553 ASIC controller, with a Serial Peripheral Interface (SPI), as a highly efficient interface between SoC processors and a MIL-STD-1553 bus.

Overview of a MIL-STD-1553 Interface

A typical implementation of a MIL-STD-1553 interface consists of a digital section (which can be implemented within an FPGA) and an analog section (which cannot be implemented within an FPGA) – refer to Figure 1. The analog section consists of a transceiver and an isolation transformer for each connection to a 1553 bus. The use of an isolation transformer is mandated by the MIL-STD-1553 standard. The transceiver is required to convert digital signals into analog signals that meet the input and output requirements of MIL-STD-1553.

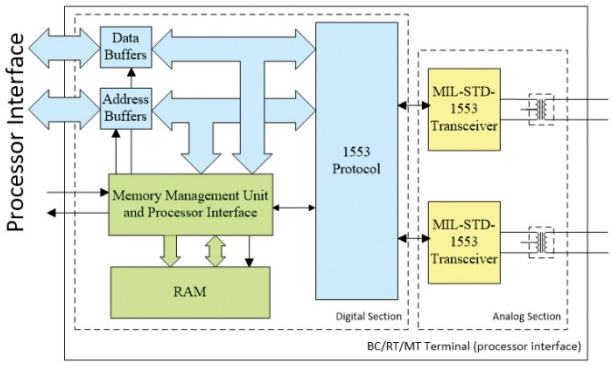

Figure 1 Block Diagram of a Typical MIL-STD-1553 Interface

The digital section of a 1553 interface consists of several major functional blocks. The protocol section is responsible for encoding and decoding the serial data stream to/from the transceiver and responding to the commands contained within that data stream. A 1553 interface to a processor typically includes a rather complex memory

Contact: Patrick Prato, Data Device Corporation
E-mail: prato@ddc-web.com **Tel:** (631) 635-6241

management unit (MMU) that controls the flow of data between a buffer memory and the 1553 bus as well as the flow of data between the buffer memory and the host processor. The MMU provides the host processor with a software interface that maintains data consistency on blocks of data exchanged in 1553 commands.

Implementations of a MIL-STD-1553 interface

ASIC Component Solutions

The most common approach to implementing a MIL-STD-1553 interface to a processor is through the use of an integrated "MIL-STD-1553 Terminal" component. These components are chip-level solutions that incorporate the required electronic circuitry in a single package. Package options for the components include a variety of form factors including ceramic, military grade packages and plastic encapsulated packages. The plastic encapsulated components tend to provide the most cost competitive solutions.

The most recent addition to DDC's MIL-STD-1553 product offering is the Nano-ACE™, which is shown in Figure 2 along with one of the required isolation transformers. The Nano-ACE is the latest evolution in the highly successful Enhanced Mini-ACE® series, which has been in operation since 1999 with more than 800 million hours of in-service history. The Nano-ACE implements a dual redundant interface to a 1553 bus consisting of a pair of transceivers, 1553 RT protocol, memory management unit and buffer RAM in a very small 7mm x 7mm QFN package. One of the features of the Nano-ACE that allows the package to be so small is the use of a serial "SPI" interface to the host processor. The SPI interface consists of four signals as opposed to a traditional parallel interface that typically includes over 40 signals. The reduction in pin count combined with additional integration enables the use of this chip scale QFN packaging technology.

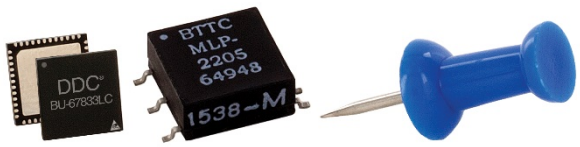

Figure 2 Nano-ACE and Separate Isolation Transformer

The size of the Nano-ACE seems compelling, but can the SPI interface handle the I/O requirements of a 1553 controller interface? DDC conducted a performance analysis of various MIL-STD-1553 implementations. DDC published a summary of this analysis in application note AN/B-59 (available on DDC's website). The results of the

analysis revealed that the 50 MHz SPI interface on the Nano-ACE provides reasonable bandwidth (6.25 Mbytes/sec) and latency (< 1µs) for a fully functioning interface between a processor and a MIL-STD-1553 bus. The App Note also estimates the host interface utilization to be less than 6% for a 1553 bus operating at 100% capacity.

FPGA + Transceivers Solutions

An alternative to the traditional component solution is to utilize an FPGA with a 1553 IP core to implement the digital portion of the 1553 interface. This solution requires the use of a dual 1553 transceiver and two isolation transformers in addition to the FPGA component since the FPGA is not capable of directly meeting the input/output characteristics of MIL-STD-1553.

An IP-based 1553 solution will occupy the exact same amount of board space (excluding the area required for the FPGA) as a component solution because the Nano-ACE and the dual transceiver are packaged in the same size QFN package.

MIL-STD-1553 SPI System on a Chip Implementation

As seen above, a MIL-STD-1553 controller ASIC with a SPI interface provides an ideal MIL-STD-1553 interface to processor solution, including SoC applications. Additionally, the use of the industry standardized SPI interface significantly reduces development and integration costs as compared to an FPGA/IP solution. Furthermore, the serial SPI signals are relatively straightforward to route (unlike high-speed serial interfaces such as PCI Express that require controlled impedances and meticulous attention to routing).

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E-mail: prato@ddc-web.com **Tel:** (631) 635-6241